

RTR ... RemoteTransmitRequest  
 SRR ... SubstituteRemoteRequest  
 IDE ... ID Extension  
 r1, r0 ... "reserved" bits  
 DLC ... DataLengthCode (0,1, ..., 8)  
 IFS ... InterFrameSpace

FIG. 1

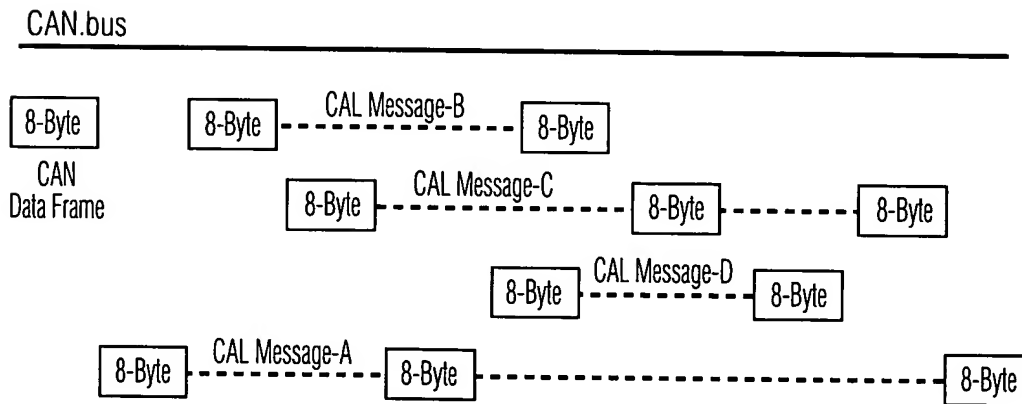


FIG. 2

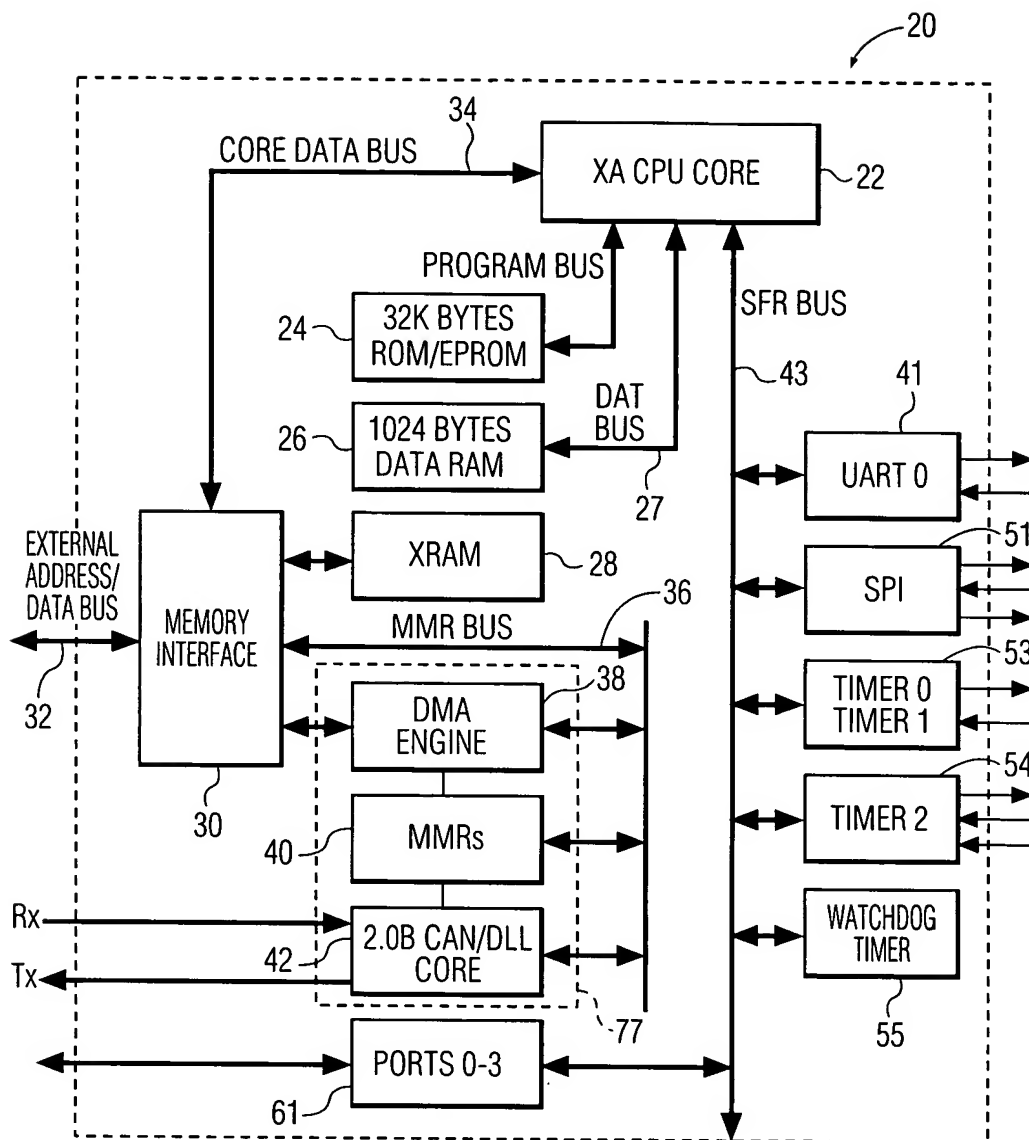


FIG. 3

MMR name	R/W?	Reset	Access	Address Offset	Description
Message Object Registers (n = 0 - 31)					
MnMIDH	R/W	x....x00b	Word only	000n4n3n2n1n0000b (n0h)	Message n Match ID High
MnMIDL	R/W	xxxxh	Word only	000n4n3n2n1n0010b (n2h)	Message n Match ID Low
MnMSKH	R/W	x....x000b	Word only	000n4n3n2n1n0100b (n4h)	Message n Mask High
MnMSKL	R/W	xxxxh	Word only	000n4n3n2n1n0110b (n6h)	Message n Mask Low
MnCTL	R/W	00000xxxb	Byte/Word	000n4n3n2n1n01000b (n8h)	Message n Control
MnBLR	R/W	xxxxh	Word only	000n4n3n2n1n01010b (nAh)	Message n Buffer Location
MnBSZ	R/W	00000xxxb	Byte/Word	000n4n3n2n1n01100b (nCh)	Message n Buffer Size
MnFCR	R/W	00xxxxxb	Byte/Word	000n4n3n2n1n01110b (nEh)	Message n Fragmentation Count
CIC Registers					
MCPLL	R/C	0000h	Byte/Word	224h	Message Complete Low
MCPLH	R/C	0000h	Byte/Word	226h	Message Complete High
CANINTFLG	R/C	0000h	Byte/Word	228h	CAN Interrupt Flag Register
MCIR	RO	0000h	Byte/Word	229h	Message Complete Info Reg.
MEIR	RO	0000h	Byte/Word	22Ah	Message Error Info Register
FESTR	R/C	0000h	Byte/Word	22Ch	Frame Error Status Register
FEENR	R/W	0000h	Byte/Word	22Eh	Frame Error Enable Register
SCP/SPI Registers					
SPICFG	R/W	0000h	Byte/Word	260h	SCP/SPI Configuration
SPIDATA	R/W	00h	Byte/Word	262h	SCP/SPI Data
SPICS	R/W	00h	Byte/Word	263h	SCP/SPI Control and Status
CCB Registers					
CANCMR	R/W	01h	Byte/Word	270h	CAN Command Register
CANSTR	R/O	00h	Byte/Word	271h	CAN Status Register
CANBTR	R/W	00h	Byte/Word	272h	CAN Bus Timing Reg. (low)
-	R/W	00h	Byte/Word	273h	CAN Bus Timing Reg. (high)
TXERC	R/W*	00h	Byte/Word	274h	Tx Error Counter
RXERC	R/W*	00h	Byte/Word	275h	Rx Error Counter
EWLR	R/W	96h	Byte/Word	276h	Error Warning Limit Register
ECCR	RO	0000h	Byte/Word	278h	Error Code Capture Register
ALCR	RO	0000h	Byte/Word	27Ah	Arbitration Lost Capture Reg.
RTXDTM	WO	0000h	Byte/Word	27Ch	RTX Data Test Mode
GCTL	R/W	0000h	Byte/Word	27Eh	Global Control Byte
MIF Registers					
XRAMB	R/W	FEh	Byte/Word	290h	XRAM Base Address
MBXSR	R/W	FFh	Byte/Word	291h	Msg. Buff./XRAM Seg. Reg.
MIFBTRL	R/W	EFh	Byte/Word	292h	MIF Bus Timing Reg. Low
MIFBTRH	R/W	FFh	Byte/Word	293h	MIF Bus Timing Reg. High

Legend: R/W = Read & Write, RO = Read Only, WO = Write Only, R/C = Read & Clear, W\* = Writable only during CAN Reset mode, x = undefined after reset.

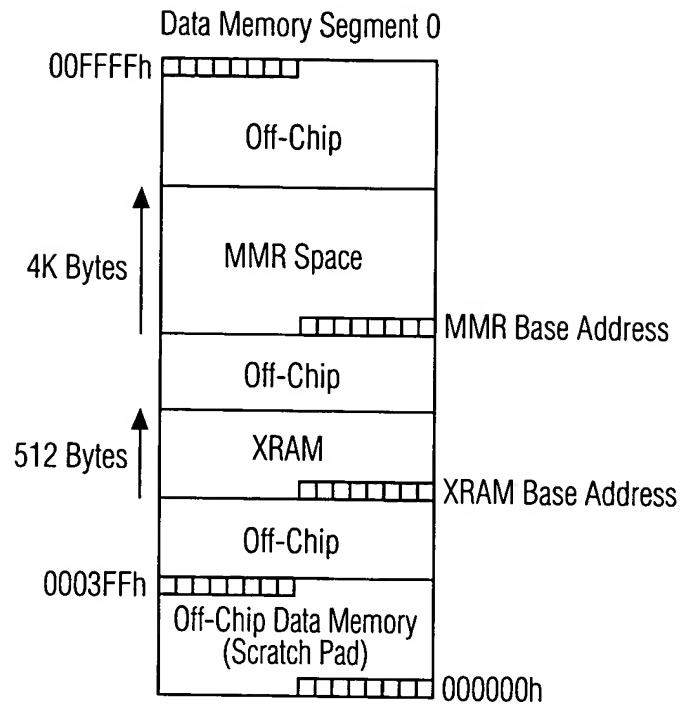


FIG. 5

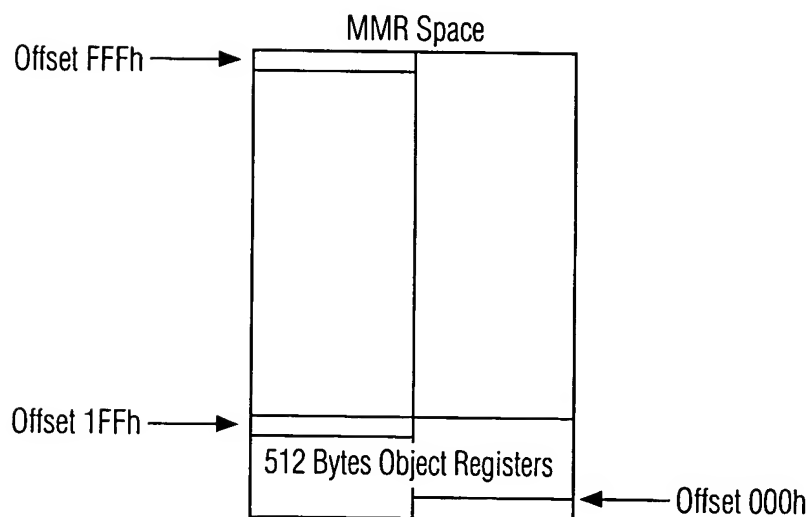


FIG. 6

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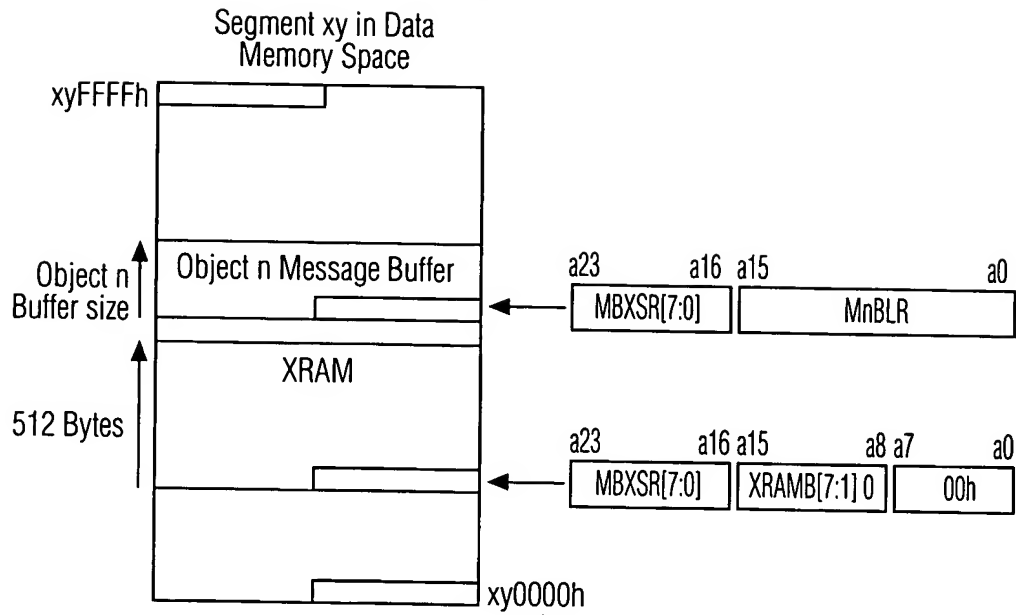


FIG. 7

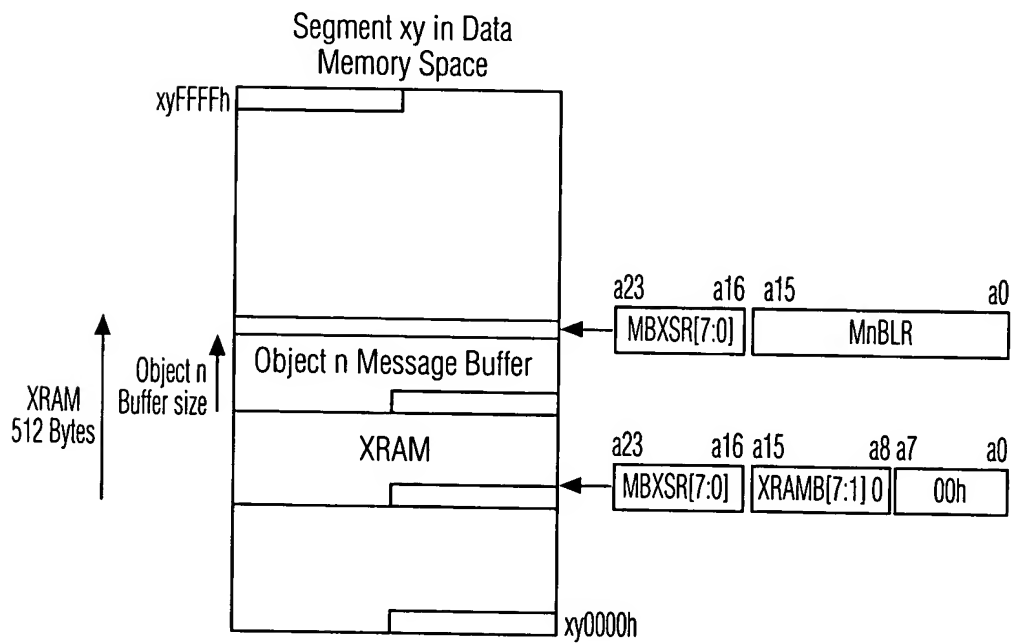


FIG. 8

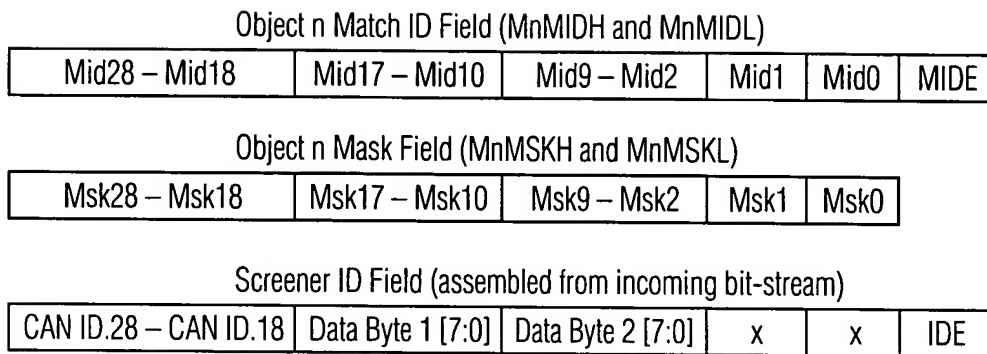


FIG. 9

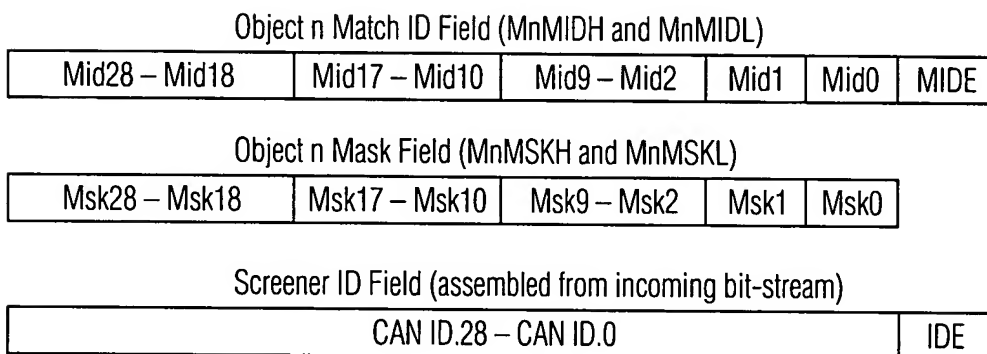


FIG. 10

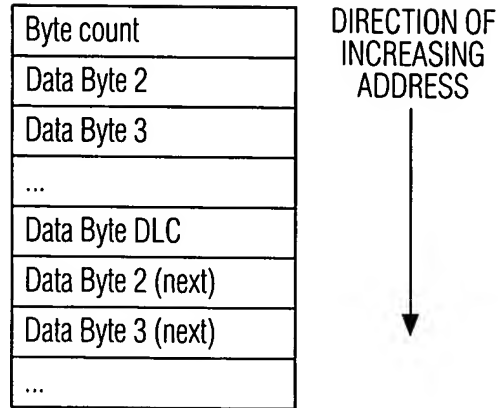


FIG. 11

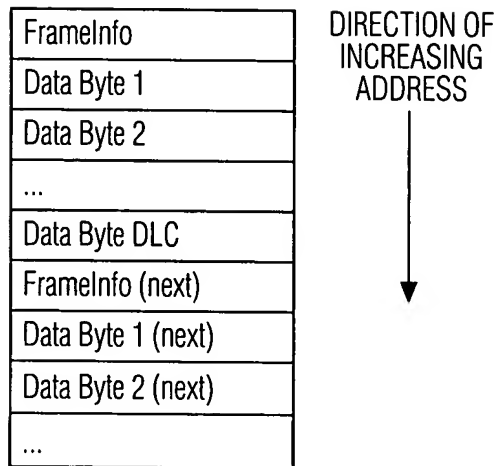


FIG. 12